

CLAIMS

We claim:

- 1 1. A circuit comprising:
 - 2 a comparator adapted to receive a first and a second input
 - 3 signal and provide a comparator output signal;
 - 4 a first register adapted to store at least one threshold
 - 5 value and at least one successive approximation register value;
 - 6 a digital-to-analog converter adapted to provide the second
 - 7 input signal to the comparator, where the second input signal is
 - 8 based on one of the threshold values or one of the successive
 - 9 approximation register values from the first register; and
 - 10 a second register adapted to store the comparator output
 - 11 signal from the comparator, wherein the circuit is adapted to
 - 12 provide threshold detection or successive approximation analog-
 - 13 to-digital conversion of the first input signal.
- 1 2. The circuit of Claim 1, further comprising a first
- 2 multiplexer adapted to select from one or more input signals to
- 3 provide as the first input signal to the comparator.

1 3. The circuit of Claim 1, further comprising:
2 a first multiplexer adapted to select from one or more
3 input signals to provide as a first output signal;
4 a sample and hold circuit adapted to store a value of the
5 first output signal and provide as a second output signal; and
6 a second multiplexer adapted to select between the first
7 and second output signal to provide as the first input signal to
8 the comparator.

1 4. The circuit of Claim 1, further comprising cycling
2 logic adapted to select the first input signal, from among a
3 number of input signals, to provide to the comparator.

1 5. The circuit of Claim 4, wherein the cycling logic is
2 further adapted to select the threshold value or the successive
3 approximation register value to provide as the second input
4 signal to the comparator.

1 6. The circuit of Claim 4, wherein the cycling logic is
2 further adapted to select a location in the second register to
3 store the comparator output signal.

1 7. The circuit of Claim 1, further comprising successive
2 approximation register logic adapted to control a value for the
3 at least one successive approximation register value based on
4 the comparator output signal.

1 8. The circuit of Claim 1, wherein the comparator output
2 signals stored in the second register provide the results from
3 threshold detection operations of the comparator.

1 9. The circuit of Claim 1, wherein the successive
2 approximation register value is a result of an analog-to-digital
3 conversion upon completion of a successive approximation analog-
4 to-digital conversion operation by the circuit.

1 10. The circuit of Claim 1, wherein the first register
2 comprises a register bank of at least two registers, with one
3 register adapted to store at least a threshold value and the
4 other register adapted to store at least a successive
5 approximation register value.

1 11. A circuit comprising:

2 a comparator adapted to receive a first and a second input
3 signal and provide a comparator output signal;

4 means for providing the first input signal to the
5 comparator; and

6 means for storing and selecting one from a number of
7 threshold values and one or more successive approximation
8 register values to generate the second input signal to the
9 comparator.

1 12. The circuit of Claim 11, wherein the means for
2 providing the first input signal includes means for selecting
3 one from among a number of input signals to provide as the first
4 input signal.

1 13. The circuit of Claim 11, wherein the means for
2 selecting one further comprises means for storing a value of the
3 one selected from the input signals to provide as the first
4 input signal to the comparator.

1 14. The circuit of Claim 11, further comprising means for
2 storing comparator output signals to provide as comparison
3 results.

1 15. The circuit of Claim 11, further comprising means for
2 updating one of the successive approximation register values
3 based on the comparator output signal to provide successive
4 approximation analog-to-digital conversion.

1 16. The circuit of Claim 11, further comprising means for
2 cycling through the input signals to provide comparator results
3 and/or successive approximation analog-to-digital conversion.

1 17. A method of providing analog-to-digital conversion and
2 threshold detection, the method comprising:

3 providing a first input signal;

4 selecting a threshold value or a successive approximation
5 register value to convert and provide as a second input signal;

6 comparing the first input signal to the second input signal
7 to provide a comparator output signal;

8 providing the comparator output signal as a threshold
9 detector result if one of the threshold values was selected; and

10 providing the comparator output signal as a comparison
11 result for successive approximation analog-to-digital conversion
12 if the successive approximation register value was selected.

1 18. The method of Claim 17, wherein the providing the
2 first input signal further comprises receiving a number of input
3 signals and selecting one to provide as the first input signal.

1 19. The method of Claim 18, wherein the receiving of the
2 input signals further comprises sampling and storing a value of
3 one of the input signals.

1 20. The method of Claim 17, wherein the comparison result
2 is used to update the successive approximation register value
3 for successive approximation analog-to-digital conversion.

1 21. The method of Claim 17, further comprising storing the
2 threshold detector results and providing as threshold comparison
3 output signals.